Sensing Voltage Transients Using Built-in Voltage Sensor

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ECE 6332 Final Project

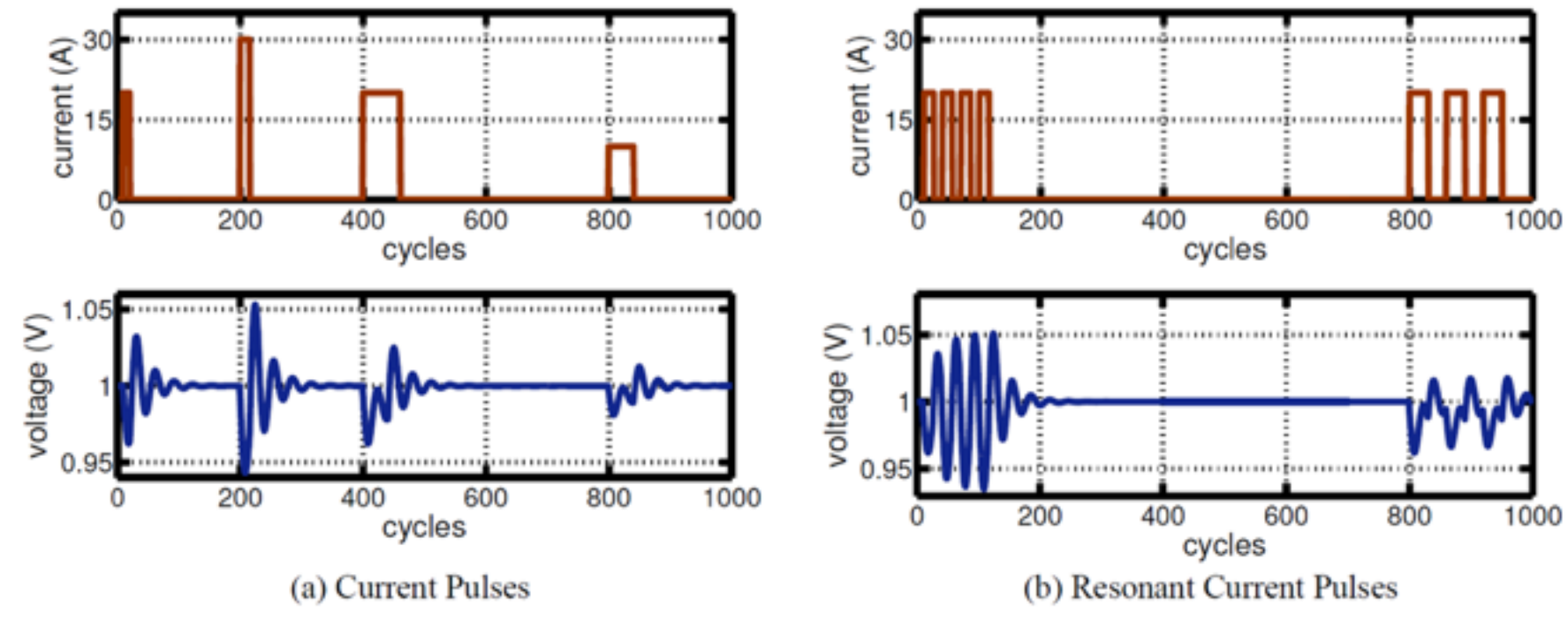
Date: December 11 2012

Outline

- 1. Introduction and Motivation
- 2. Related Work
- 3. Design the Voltage Sensor
- 4. Simulation Results
- 5. Layout and Post-Layout Simulation

Voltage Transients

- Fluctuations in voltage due to inductive noise, also called voltage emergencies, Ldi/dt noise, voltage droops.



(a) Current Pulses

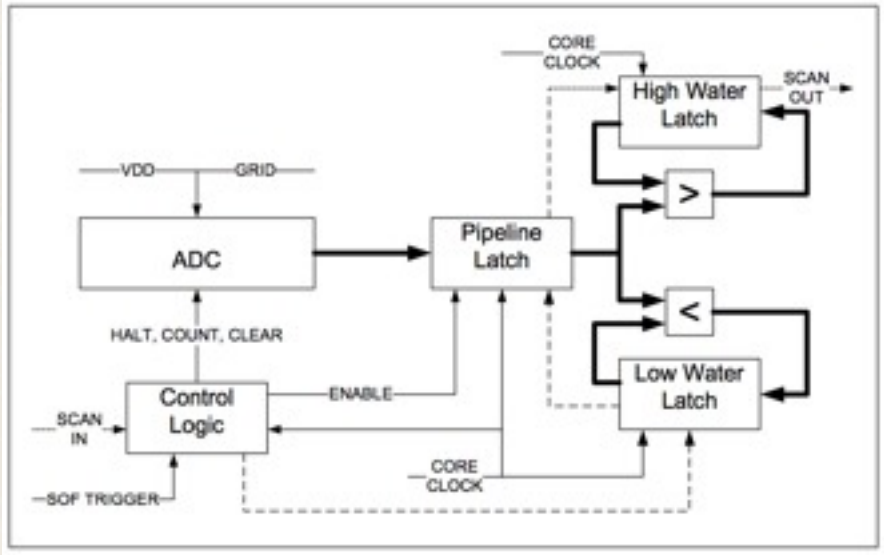
(b) Resonant Current Pulses

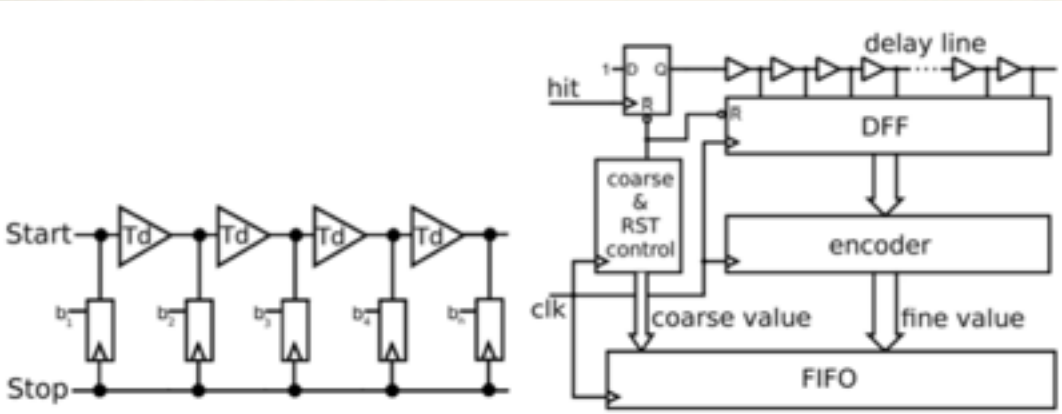
Motivations

- Voltage transient characteristics are not fully understood.
  - Time scale, frequency and amplitude?
- Lack of sensors that can effectively detect the voltage transients.
- How to protect ICs against voltage transients?
- Motivation: to better study the voltage transients in modern ICs, we investigated a purely digital voltage sensor that can detect voltage transients effectively.

Previous Work

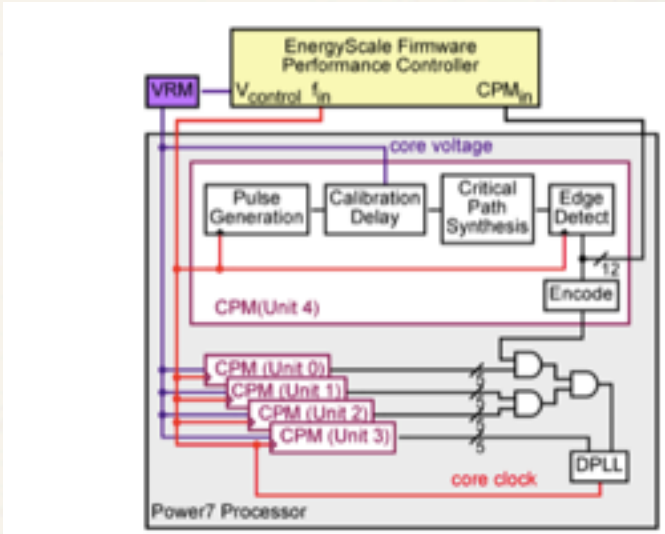
- **Intel Droop Detector**
- **Time-to-Digital Converter**
- **IBM Critical Path Monitor**



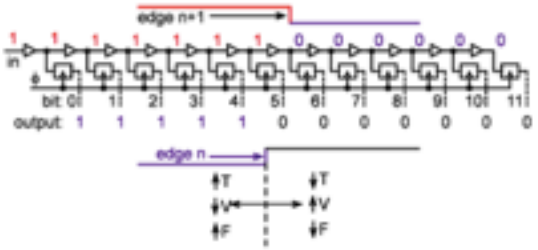


(a) Buffer Delay Line schematic

(b) Multi-stage Architecture with Delay Line



A) CPM block diagram for 1 processor core.



B) Edge detector in CPM.

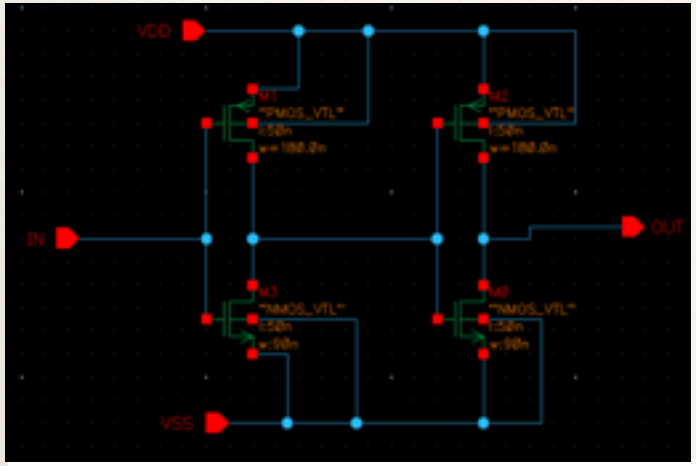
Design the Voltage Sensor

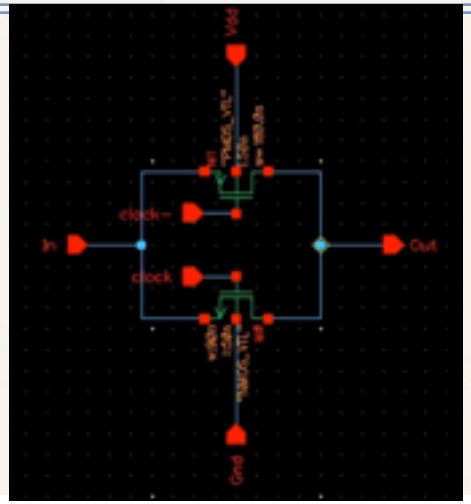
- Two key components:
  - Voltage sensitive delay line
    - Delay line is a chain of basic delay gates.
    - The delay of CMOS gates change with voltages (higher voltage, lower delay, and vice versa).
    - The more sensitive to voltage, the better.
  - Time-to-Digital Converter
    - The less sensitive to voltage, the better.

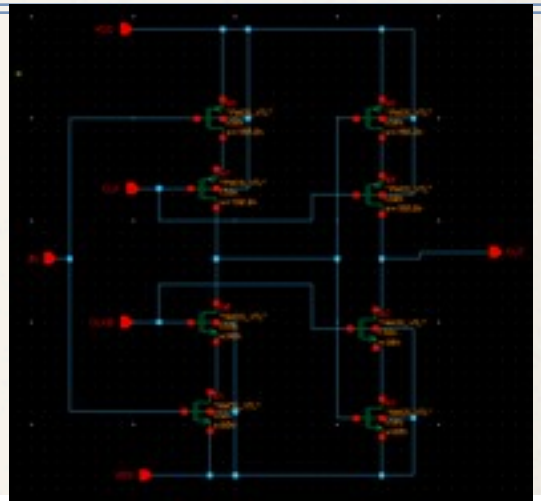
Design Specification

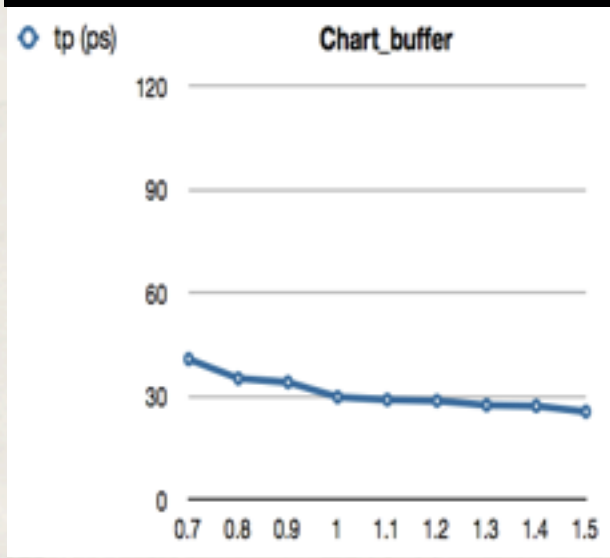
- Nominal voltage: 1.1 volts (45nm FreePDK library)
- Minimum voltage: 0.8 volts
- Maximum voltage: 1.4 volts
- Measure range of the sensor: 0.6 volts
- Resolution: 1bin/10mV
- Number of bins: 64
- Actual measure range: 640mV

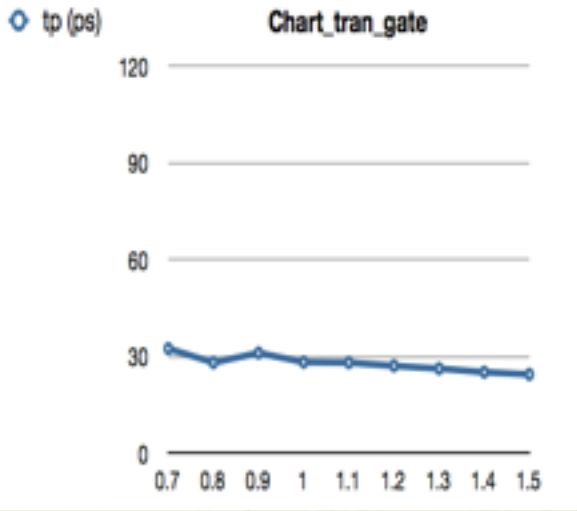
Basic Delay Gates

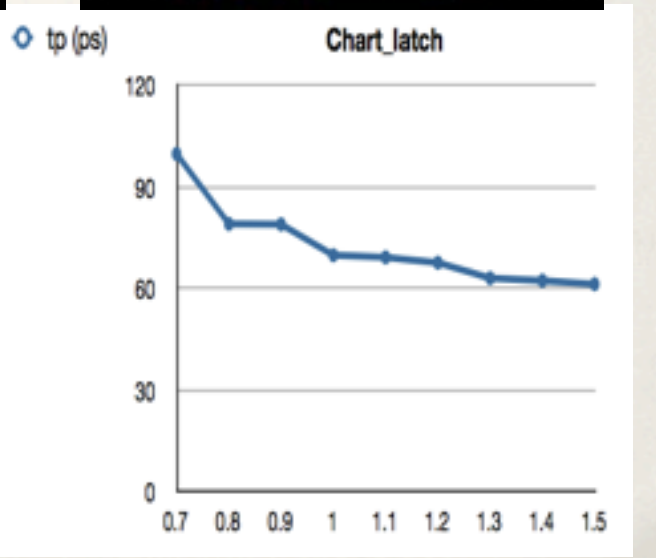










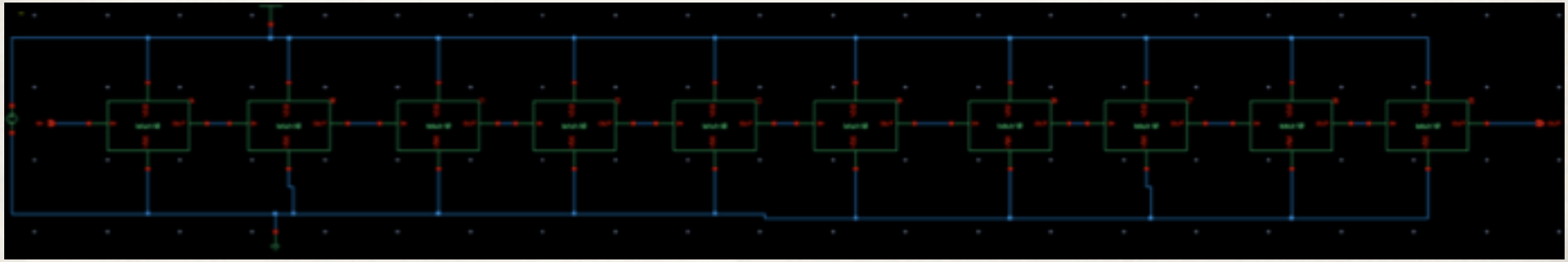


Design the Delay Line

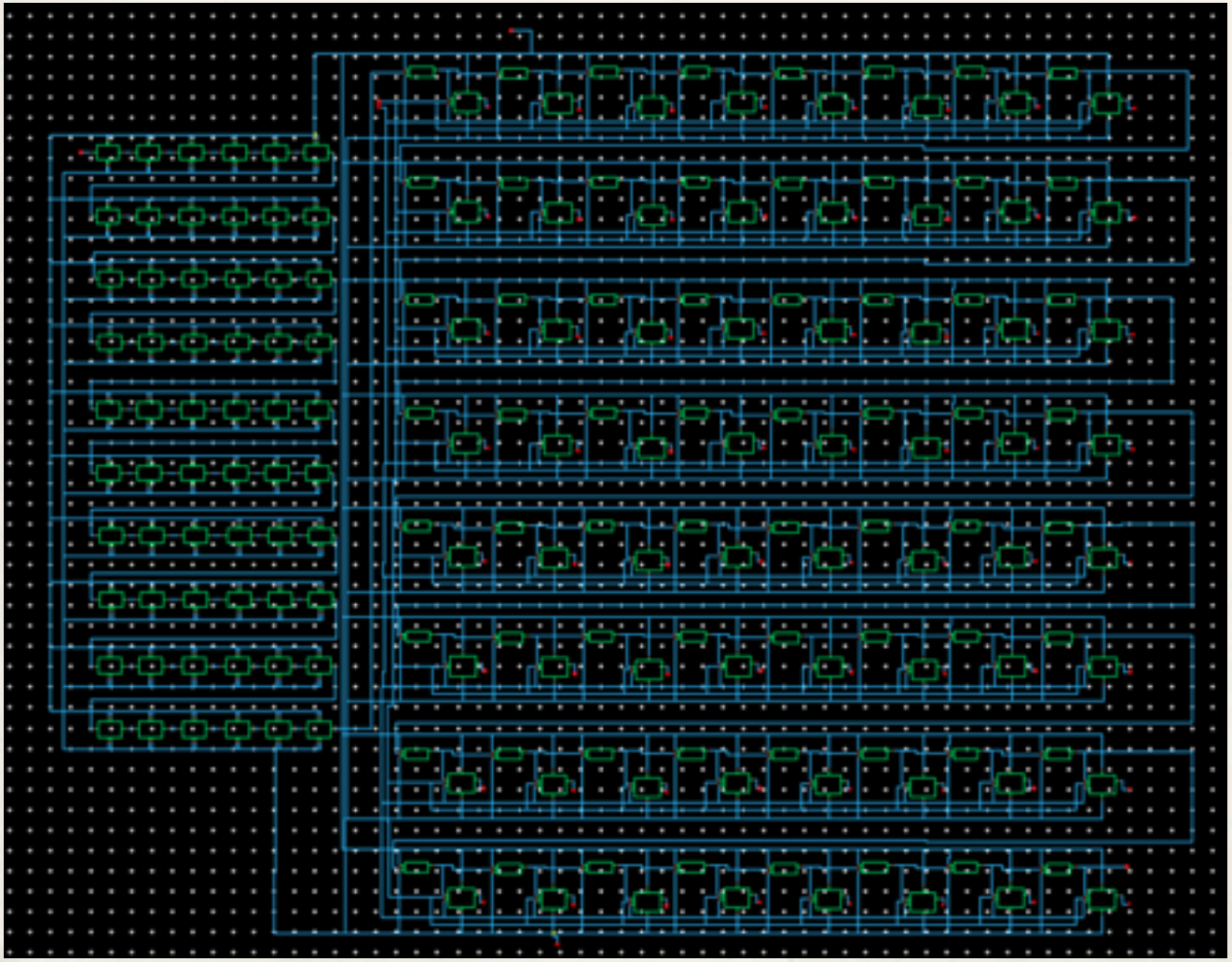
buffer			
voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
0.7	40.7	40.8	40.75
0.8	35.5	34.8	35.15
0.9	32.8	35.3	34.05
1	29.6	29.9	29.75
1.1	29.3	28.6	28.95
1.2	29	28.3	28.65
1.3	27.2	27.6	27.4
1.4	26.7	27.6	27.15
1.5	25	26	25.5

latch			
voltage (V)	rising time (ps)	falling time (ps)	tp (ps)
1.5	60.6	62.36	61.48
1.4	59	66	62.5
1.3	64.6	61.9	63.25
1.2	67.3	68.31	67.805
1.1	70	68.78	69.39
1	69.7	70.35	70.025
0.9	80.4	77.87	79.135
0.8	78.5	80.05	79.275
0.7	100.1	99.79	99.945

	number of Transistors	delay/voltage	number of gates needed
buffer	4	1.333ps/100mV	64
latch	8	2.542ps/100mV	114

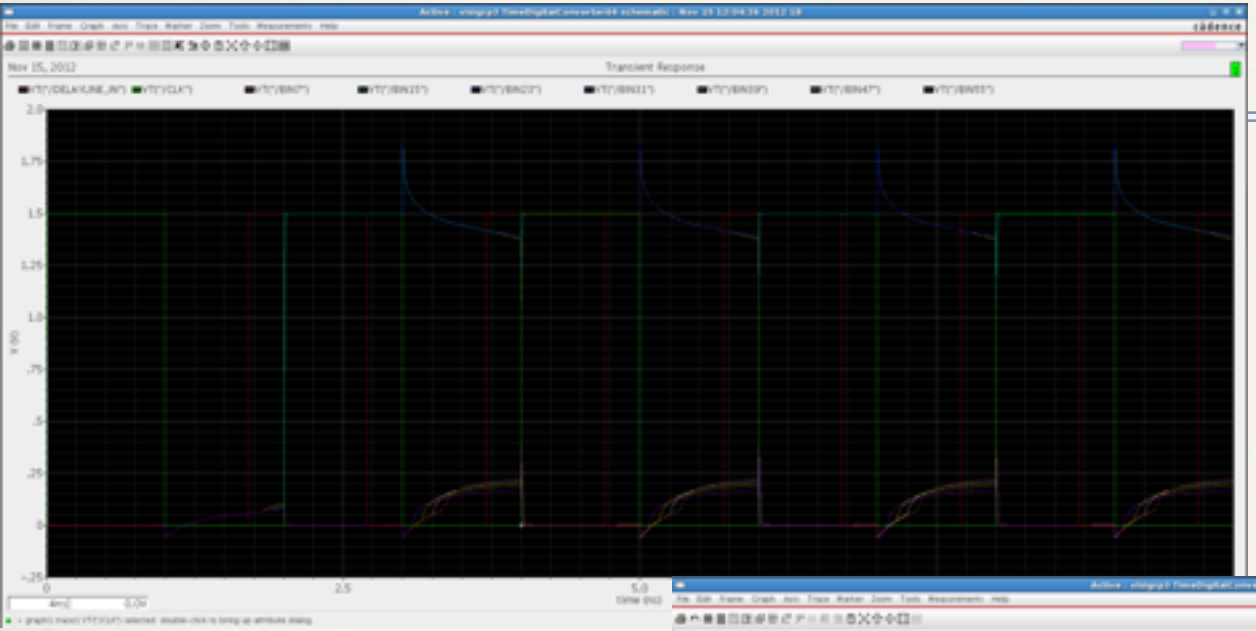


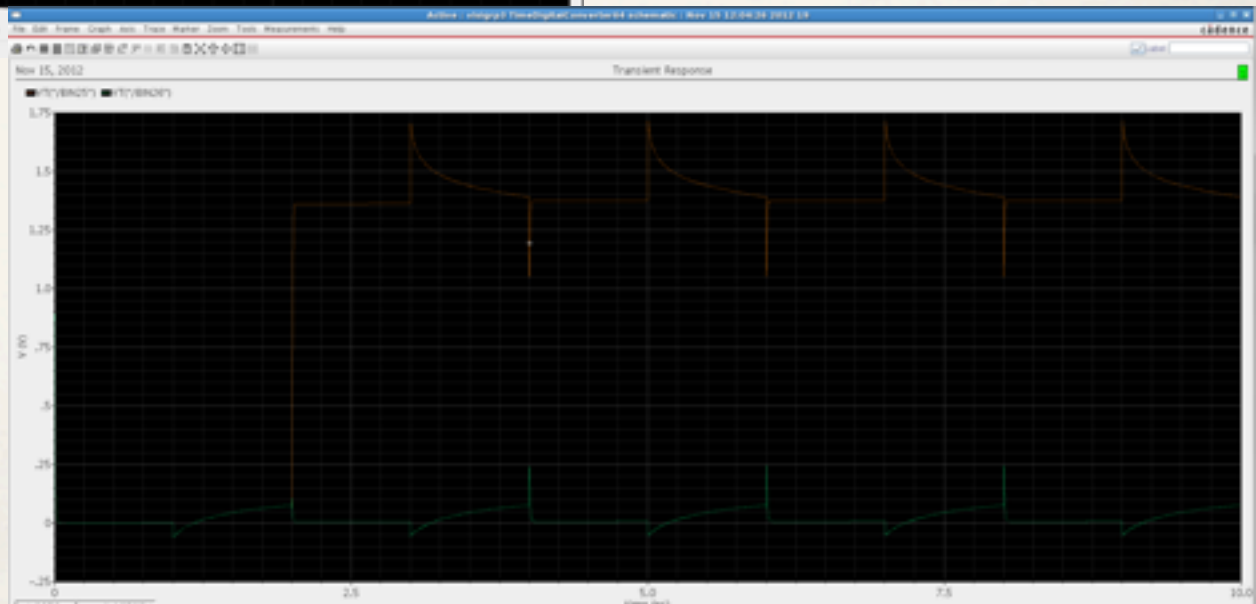
Design the TDC



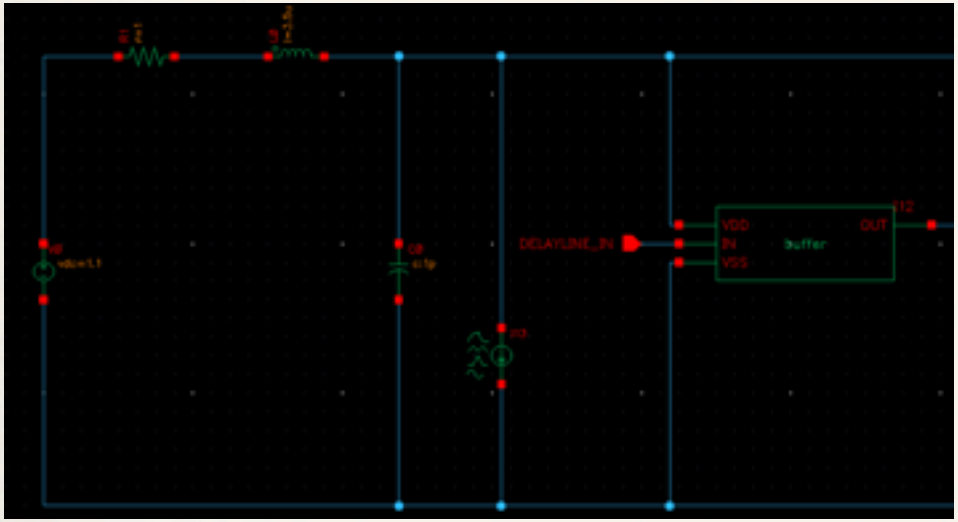
- Left side is the delay line.
- Right side is the TDC.

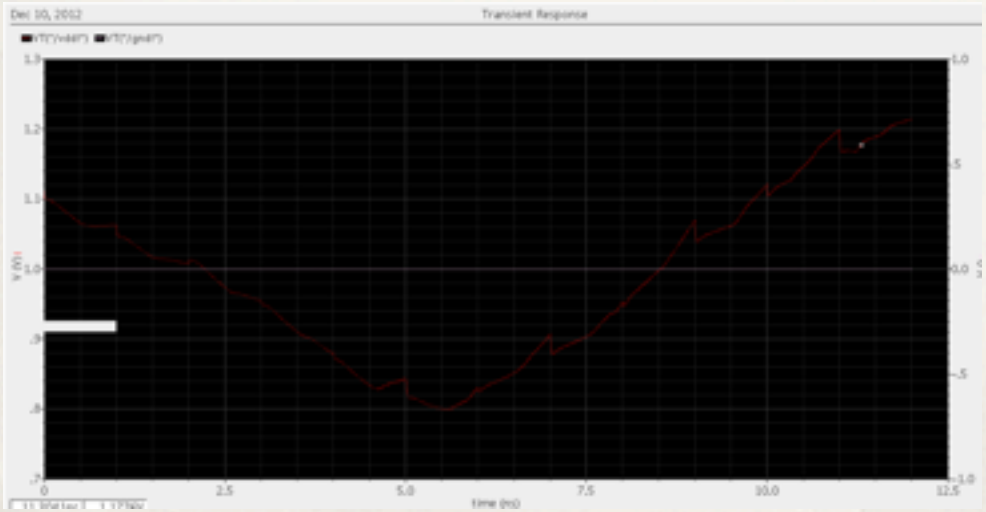
Simulation Results





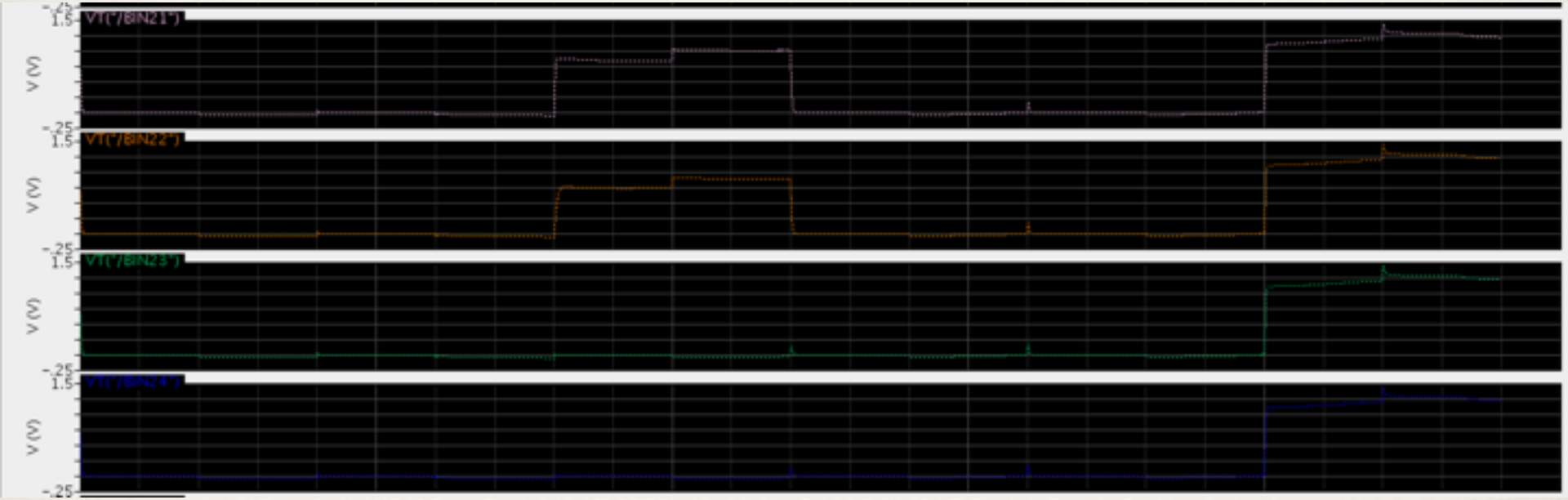
Model the Power Network



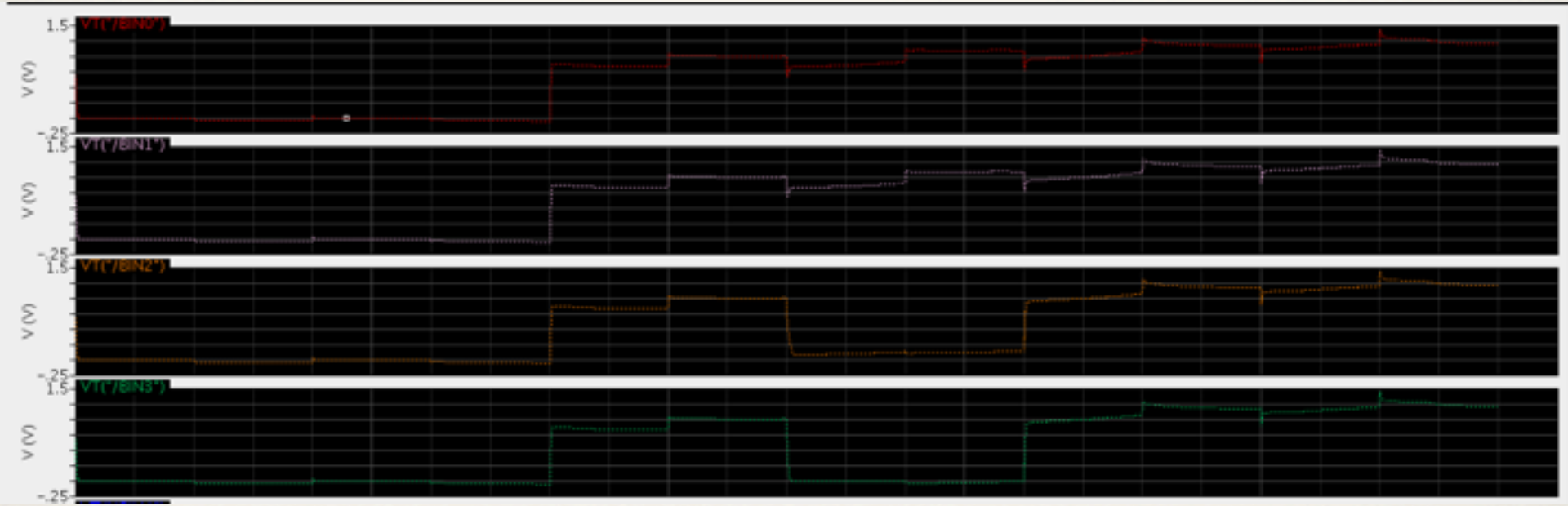


- Resistance
- Inductance
- Capacitance
- Voltage supply
- Load (modeled as current source)

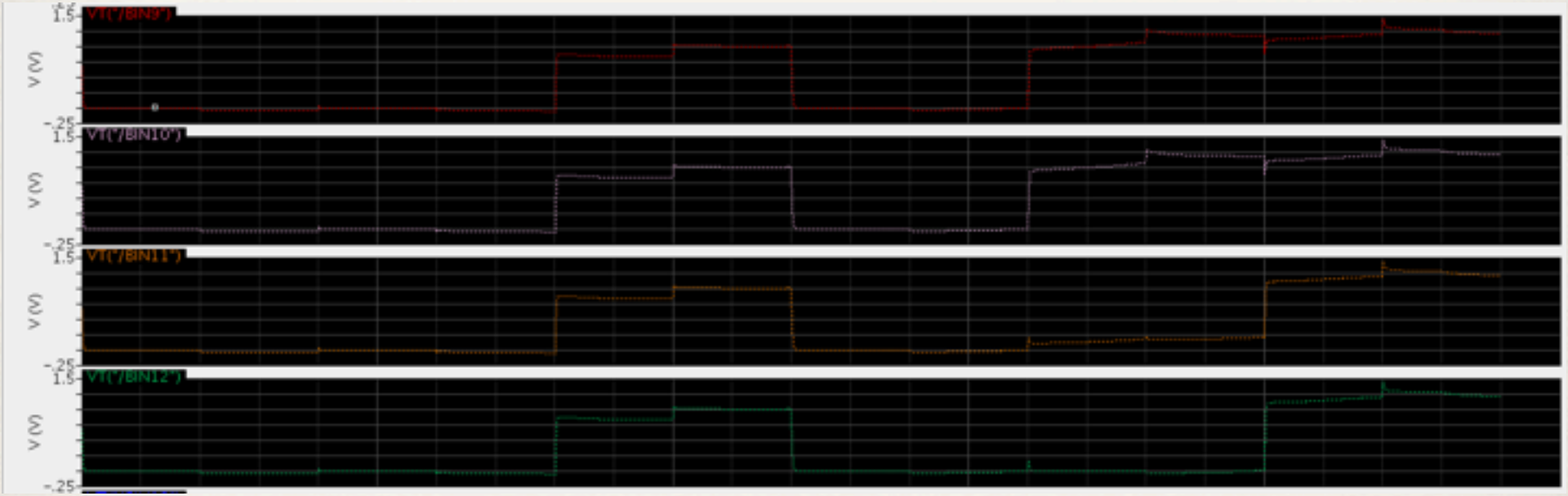
Simulation Results



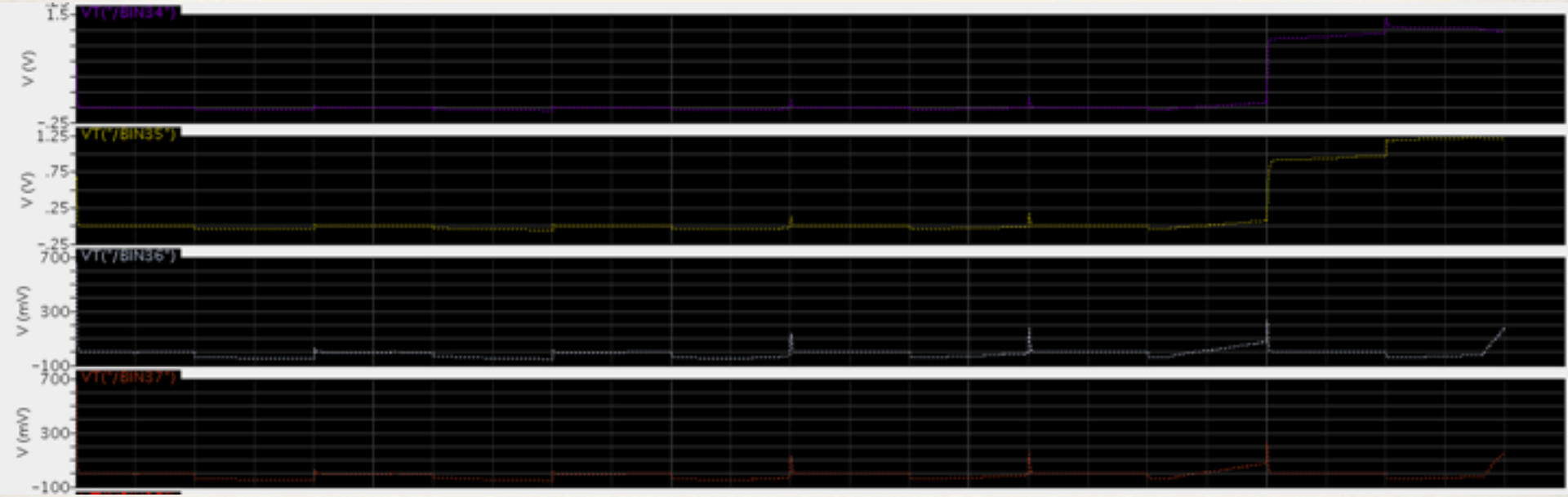
Simulation Results



Simulation Results



Simulation Results

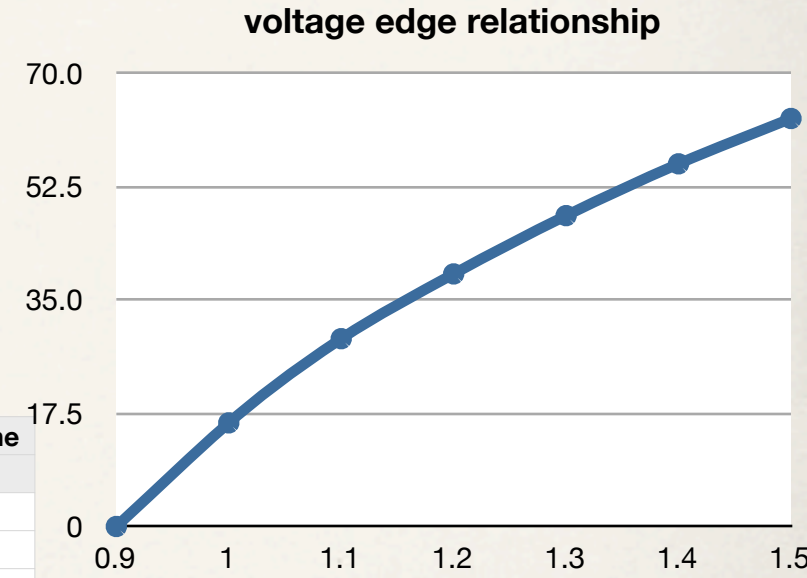


Simulation Results

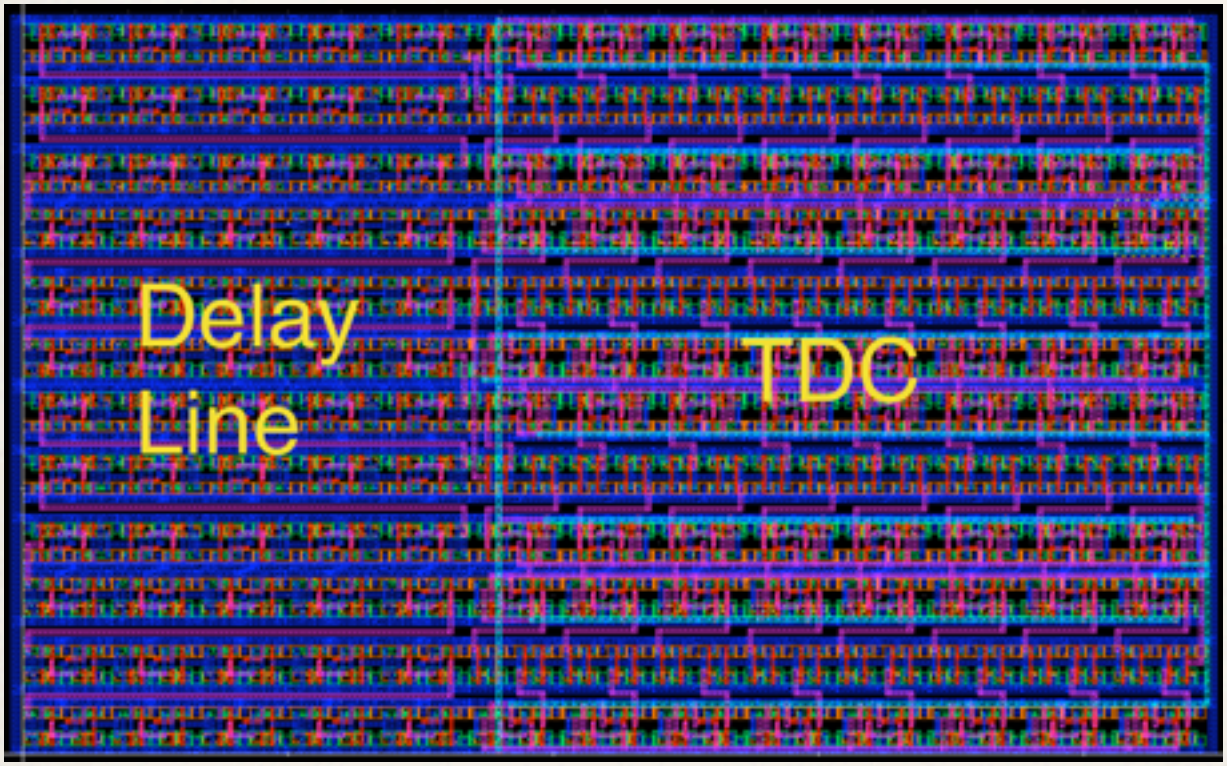
delay line with 100 open latches				
voltage (V)	**rising time (ns)**	**falling time (ns)**	**tp (ns)**	**delay/voltage (ns/100mV)**
0.7	4.717	4.707	4.712	0.46763
1.1	2.828	2.855	2.8415	
1.5	2.334	2.326	2.33	0.29775

Delay of TDC				Delay of TDC Delay Line
voltage (V)	**transition bin**	**No. of shift bins**	**bin/voltage**	**in: 4.06n**
0.7	23,24	14	1bin/29mV	out: 5.13n
1.1	37,38	0		delay: 1.07n
1.5	43,44	6	1bin/67mV	maximum freq.: 467MHz

Delay of Voltage Sensor					
voltage (V)	**transition bin**	**No. of shift bins**	**bin/voltage**	**ideal bin No.**	**current delay**
0.9	0,1	16	1bin/6.25mV	15	1.9n
1.0	16,17	13	1bin/7.69mV	31	
1.1	29,30	0		44	1.7n
1.2	39,40	10	1bin/10mV	54	
1.3	48,49	9	1bin/11mV	63	
1.4	56,57	8	1bin/12.5mV		
1.5	63,64	7	1bin/14mV		



Layout



- LVS successful
- Parasitics extracted
- Post-layout simulation
- Total area:
  22.5675*13.9850 um2

The end!

Thanks!